

signal opens the buffer gates that connect the BUS allowing the PC contents to flow into the adder and the Sum_{in} signal store the incremented address in the Sum Register.

2. At time T_1 , the control signals Sum_{out} and PC_{in} are activated. The Sum_{out} Signal opens the buffer gates that connect to the BUS allowing the Sum-Register contents to flow into the BUS and the PC_{in} signal allows the incremented address into the PC Register.

The Data Registers A and B each store 4-bits of data. During execution of the instruction MovAB or MovBA, data of the source register flows through the BUS into the destination register. During execution of IncA or IncB, data of the specified register flows through the BUS to the adder and back to the register through the BUS.

RAM 305 contains sixteen 4-bit data locations and it can store sixteen instructions. During programming, one manually specifies these instructions and their RAM locations (i.e., the instruction address) via the switches. During program execution, within each instruction cycle, RAM receives an instruction address from the PC and delivers the 4-bit instruction to the Instruction Decoder.

Instruction Decoder 306 has a circuit that decodes a 4-bit instruction to activate one of the four instruction signals that goes into the Control Signal Encoder. Control Signal Encoder 302 maps the incoming instruction signals and timing signals into control signals which trigger sub-operations within an instruction cycle. The Program Counter is incremented via the first two timing signals of the instruction cycle: the signal T_0 activates PC_{out} and Sum_{in} , and the signal T_1 activates Sum_{out} and PC_{in} . An instruction is executed during the time T_2 and T_3 time steps of the instruction cycle. For example,

the instruction IncA is executed via activating the control signals A_{out} and Sum_{in} at T_2 , and activating the signals A_{in} and Sum_{out} at T_3 . One notes that the contents of the Program Counter which is incremented during the first two timing signals stays the same during the rest of the instruction cycle. Therefore, all through T_2 and T_3 , RAM output pins contain the same instruction and the Instruction Decoder 306 continuously feeds into the Control Signal Encoder the signal for this instruction.

To operate the teaching aid, one enters his or her program into RAM 305 manually before execution using the data and address switches. As Figure 4 illustrates, each 4-bit memory location for storing an instruction has a 4-bit address. These addresses range from 0000 to 1111. To write into RAM, the student specifies the memory location via the address switch, specifies the instruction via the data switch, and manually sends to RAM a write signal. The four pins of the data switch connects to RAM's data input pins and the four pins of the address switch connect to RAM's address pins (not shown).

While only one embodiment of this invention has been shown and described in detail it will be obvious to those of ordinary skill in the art to devise other modifications and changes without departing from the scope of the appended claims. For example, one can choose to write one's own codes for the given instructions. To do this, one will have to redesign the wiring in the Instruction Decoder and the Control Signal Encoder accordingly using the design shown herein as an example.

Likewise, the signals T_0 , T_1 , T_2 and T_3 used in this example can

be replaced with other timing signals of the instruction cycle. The chips shown in Figure 3 can obviously be arranged differently and by adding more breadboards to the package, one can enhance the Arithmetic and Logic Unit by including other chips for division, multiplication subtraction, etc. One can also provide for a larger instruction set to implement those added functions. One could also implement interrupt processing and connect input devices to this mechanism. One can also replace the RAM with a larger RAM, modify the Ram access mechanism (e.g., by including MAR, MBR, and IR registers) and modify the instruction format to support a stack machine or a 1-address, a 2-address, or a 3-address machine. One can also replace the 4-bit simple computer with an 8-bit simple computer.



1. A programmable 4-bit simple teaching computer, said computer comprising
a central memory section,
a central processing unit, and
an input /output section allowing for manual programming of the
computer.

whereby said computer can be used to teach students the basic architecture of
computers.
2. A programmable teaching computer as in claim 1 wherein said computer is
designed to accommodate a maximum of sixteen instructions but implements four
basic machine language instructions.
3. A programmable teaching computer as in claim 2 and wherein said computer
includes light emitting diodes so that students can follow visually the operation of
the simple computer.
4. A programmable teaching computer as in claim 1 wherein said memory includes
a RAM capable of storing only sixteen 4-bit instructions.
5. A programmable teaching computer as in claim 1 wherein said Central
Processing Unit has a arithmetic logic unit having only the add function and no other.
6. A programmable teaching computer as in claim 5 wherein the memory of said
computer includes a RAM capable of storing only sixteen 4-bit instructions.

7. A programmable teaching computer as in claim 1 wherein said Central Processing Unit contains an Arithmetic Unit containing only an adder and a Sum Register.

8. A programmable teaching computer as in claim 1 wherein said computer also includes control circuit functions including a clock, a timing signal generator, an instruction fetch and an instruction execution function.

9. A programmable teaching computer as in claim 1 wherein said computer also includes two Central Processing Unit Registers, both of which are 4-bit register.

10. A programmable teaching computer as in claim 1 wherein said computer's components are all arranged on four bread boards which are interconnected.

11. A programmable teaching computer as in claim 1 and including a Timing Signal Generator with a clock, counter, decoder and inverter.

12. A programmable teaching computer as in claim 1 and including a Control Signal Generator having two AND/OR gate chips.

13. A programmable teaching computer as in claim 1 and including two Registers With output buffers.

14. The programmable teaching computer as in claim 1 wherein said Memory includes a RAM connected to a Program Counter which has an Output Buffer.

15. The programmable teaching computer as in claim 14 wherein an Instruction Decoder is also connected to said RAM.

16. A programmable teaching computer as in claim 1 wherein said computer components are positioned on four bread boards.

17. A programmable teaching computer as in claim 16 wherein a first breadboard contains a Timing Signal Generator.

18. A programmable teaching computer as in claim 17 wherein a second breadboard contains a Program Counter and an Arithmetic Unit.

19. A programmable teaching computer as in claim 18 wherein a third breadboard contains two Data Registers and a Bus consisting of four parallel conductors used by the chips for interchanging data.

20. A programmable teaching computer as in claim 19 wherein a fourth breadboard contains a RAM and an Instruction Decoder.

21. A programmable teaching computer as in claim 19 wherein a Control Signal Generator is located on the second, third and fourth breadboard.

22. A computer kit for use in teaching computer architecture and programming, said kit containing a set of integrated circuit chips for constructing a Central Processing Unit, an input/output component and a Memory, said kit also containing at least four breadboards having power strips.

23. A computer kit as in claim 22 wherein said Memory contains sixteen 4-bit data locations.

24. A computer kit as in claim 22 and including integrated circuit chips, power supply, switches, wire, LEDs, resistors, a capacitor and a lab instruction manual.